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EXAMINER	
HUA, LY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,295	HAZAMA, KATSUKI	
	Examiner	Art Unit	
	Ly V. Hua	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *November 12, 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,7 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *8-25 and 33-42* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/931,519* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Restriction to one of the following four Groups of inventions is required under 35 U.S.C. 121:

Group I. Claims 6, 7, claims 26-29, claim 30, claim 31 and claim 32, drawn to the following, classified in class 714, subclass 701 (data error-handling/**data-formatting**-to-improve-error-detection-correction-capability:

i.6 A computer readable medium storing program code for causing a computer to write data of bits in a semiconductor device having a plurality of multilevel memory cells, each cell storing at least three levels of data each, comprising:

(1) first program code means for entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, **the first and the second data being coded by a coding method**; and

(2) second program code means for **arranging the first and the second data bits such that at least a bit of an N-order of the first data bits and a bit of the N-order of the second data bits are stored in one of the cells**, N being an integral number.

ii. 26. A semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the semiconductor device comprising a bit disperser for **dispersing bits over the plurality of multilevel memory cells** to store the bits therein, **the bits constituting at least one code data coded by a coding method** to be stored in the cells.

iii.30. A computer readable medium storing program code for causing a computer to store data in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, comprising a program code means for **dispersing bits over the plurality of multilevel memory cells** to store the bits therein, **the bits constituting at least one code data coded by a coding method** to be stored in the cells.

iv.31 A method

(1) of writing

(a) at least one **code data**

(i) **coded by a coding method**

(b) in a semiconductor device

(i) having a plurality of multilevel memory cells,

1) each cell storing one of at least three levels of data each,

(2) the method comprising the step of

(a) **dispersing**

(i) **bits constituting the code data**

(ii) **over the plurality of multilevel memory cells**.

v.32 A computer readable medium storing program code for causing a computer to write at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, comprising the program code for **dispersing bits constituting the code data over the plurality of multilevel memory cells**.

Group II. Claims 33-36, drawn to the following, classified in class 711, subclass 103 (**storage-accessing-and-control**/specific-memory-component/**programmale-read-only-memory**):

vi.33 A semiconductor device

(1) comprising:

(a) inputting means for inputting a logical address;

(b) converting means for converting the logical address into a physical address;

(c) a plurality of multilevel memory cells

(i) arranged so as to correspond to physical addresses,

(ii) each cell storing at least three levels of data each,

1) the data being expressed by data components of two-dimension or more;

(d) **controlling means for**

(i) **selecting one of the cells corresponding to the physical address** and

(ii) **designating**

1) **one of the data components**

2) **in accordance with the logical address;**

and

(e) outputting means for outputting the designated data component,

(2) wherein the semiconductor device

(a) has

(i) a judging value

1) for specifying,

I by a one-time specifying operation,

II at least one of the data components,

and

(b) **the controlling means,**

(i) **when the logical address is included in an address space A1 that corresponds to an address space including the physical address,**

(ii) **specifies the designated data component means of the judging value to produce the specified data from the outputting means.**

Group III. Claims 37-39 and claims 40-42, drawn to the following, classified in class 365, subclass 189.09 **(Read-Circuit/Including-reference-voltage-generator)**:

vii.37. A method

(1) of reading data

(a) stored in a semiconductor device

(i) having at least one multilevel memory cell

1) provided so as to correspond to a physical addresses converted from an input logical address,

2) the cell having a control gate, a source and a drain,

3) the cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more,

(2) comprising the steps of:

(a) **preparing** a judging value for specifying at least one of the data components; and

(b) **applying**

(i) **a voltage corresponding to the judging value**

(ii) **to the control gate**

(iii) to determine whether a current flows between the source and the drain

(iv) when the logical address is included in an address space A1 that corresponds to an address space including the physical address.

viii.40 A computer readable medium

(1) storing program code

(2) for causing a computer to read

(a) data

(i) stored in a semiconductor device

1) having at least one multilevel memory cell

I provided so as to correspond to a physical addresses converted from an input logical address,

II the cell having a control gate, a source and a drain,

III the cell storing at least three levels of data each,

2. the data being expressed by data components of two-dimension or more;

(1) comprising:

(a) first program code means

(i) for **preparing a judging value for specifying** at least one of the data components; and

(b) second program code means

(i) for **applying**

1) **a voltage corresponding to the judging value to the control gate**

2) to determine whether a current flows between the source and the drain

3) when the logical address is included in an address space A1 that corresponds to an address space including the physical address.

Group IV. Claims 8-13, 14-15, and 20-21, claims 16-17, and 22-23, and claims 18-19, and 24-25, drawn to the following, classified in class 714, subclass 763 (digital-data-error-correction/**correction-by-block-code/memory-access**):

i. 8 A semiconductor device comprising:

(1) converting means for converting a logical address into a physical address;

(2) a plurality of multilevel memory cells arranged so as to correspond to a physical address space including the physical address, each cell storing 2^n levels of data each expressed by n (n => 2) number of bits (X1, X2, ..., Xn);

(3) **judging means for judging whether a logical address space including the logical address matches the physical address space**;

(4) **specifying means for specifying the most significant bit** X1, by one-time specifying operation, by means of a reference value when the logical address space matches the physical address space; and

(5) **outputting means for outputting the specified bit from one of the cells corresponding to the physical address**.

ii.14 A method

(1) of reading

(a) n (n => 2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(c) arranged so as to correspond to a physical address space,

(d) each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) **judging whether a logical address space including the logical address matches the physical address space;**

(c) **specifying the most significant bit X1**, by

(i) one-time specifying operation, by means of a reference value

(ii) when judged that the logical address space matches the physical address space; and

(d) **outputting the specified bit from one of the cells corresponding to the physical address.**

iii. 20. A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

iv.16 A method

(1) of reading

(a) n (n => 2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(i) arranged so as to correspond to a physical address space,

(ii) each cell having at least one transistor,

(iii) each cell storing 2 n levels of data each expressed by the bits (X1, X2, ..., and Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) judging whether a logical address space including the logical address matches the physical address space;

(c) specifying the most significant bit X1 by

(i) applying

1) a predetermined reference voltage

2) to a gate of the transistor

3) to determine whether a current flows between a source and a drain of the transistor

4) when the logical address space matches the physical address space; and

(d) outputting the specified bit from one of the cells corresponding to the physical address.

v.22 A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit Xl by applying a reference voltage to a gate of the transistor when the logical address space matches the physical address space to determine whether a current flows between a source and a drain of the transistor; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

vi.18 A method

(1) of reading

(a) n (n => 2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(i) arranged so as to correspond to a physical address space,

(ii) each cell having at least one transistor,

(iii) each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., and Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) judging whether a logical address space including the logical address matches the physical address space;

(c) specifying the most significant bit X1 by

(i) comparing

1) an output voltage of the transistor corresponding to

2) the most significant bit with a reference voltage

3) when the logical address space matches the physical address space; and

(d) outputting the specified bit from one of the cells corresponding to the physical address.

vii.24 A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit X1 by comparing an output voltage of the transistor corresponding to

the most significant bit with a reference voltage when the logical address space matches the physical address space; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

3. The inventions are distinct, each from the other because of the following reasons: Inventions of Group I and II are related as sub-combinations disclosed as usable together in a single combination. The sub-combinations are distinct from each other if they are shown to be separately usable. In the instant case, the invention of Group I has separate utility such as writing data into a memory device and the invention of Groups II and III does not has a utility of such writing, but rather it has a utility of reading data from the memory device. See MPEP § 806.05(d).

4. Inventions of Groups II, III and IV are related as combination and sub-combination. Inventions in this relationship are distinct if it can be shown that:

a. the combination as claimed does not require the particulars of the sub-combination as claimed for patentability, and

b. that the sub-combination has utility by itself or in other combinations (MPEP § 806.05(c)).

5. In the instant case:

a. The combination as claimed does not require the particulars of the sub-combination as claimed because:

i. The invention of Group II, which is supposed to be operative by the recitation itself, does not require the preparing and the applying steps of the invention of Group III;

ii. The invention of Group III, which is supposed to be operative by the recitation itself, does not require the specifying step of the invention of Group IV; and

b. The sub-combination of Group III has separate utility such as for preparing a judging value and applying a voltage corresponding to the judging value that are not necessarily used in a semiconductor having the controlling mean of the invention of Group II.

c. The sub-combination of Group IV has separate utility such as for specifying the most significant bit not necessarily used in the semiconductor having the controlling means of the invention of Group II.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

7. Because these inventions are distinct for the reasons given above and (1) the search required for Group I is not required for Group II and (2) the search required for Group II is not required for Group III, restriction for examination purposes as indicated is proper.

8. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

SPECIES OF THE CLAIMED INVENTION WITHIN GROUP IV

9. This application contains claims directed to the following patentably distinct species of the claimed invention:

a. First species (i.e., having a feature of specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space):

i.8 A semiconductor device comprising:

(1) converting means for converting a logical address into a physical address;

(2) a plurality of multilevel memory cells arranged so as to correspond to a physical address space including the physical address, each cell storing 2^n levels of data each expressed by n (n=>2) number of bits (X1, X2, ..., Xn);

(3) judging means for judging whether a logical address space including the logical address matches the physical address space;

(4) specifying means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when the logical address space matches the physical address space; and

(5) outputting means for outputting the specified bit from one of the cells corresponding to the physical address.

ii.14 A method

(1) of reading

(a) n (n =>2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(c) arranged so as to correspond to a physical address space,

(d) each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) judging whether a logical address space including the logical address matches the physical address space;

(c) specifying the most significant bit X1, by

(i) one-time specifying operation, by means of a reference value

(ii) when judged that the logical address space matches the physical address space; and

(d) outputting the specified bit from one of the cells corresponding to the physical address.

iii. 20. A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

b. First species (i.e., having a feature of specifying the most significant bit X1 by applying a predetermined reference voltage to a gate of the transistor to determine whether a current flows between a source and a drain of the transistor when the logical address space matches the physical address space):

i.16 A method

(1) of reading

(a) n (n => 2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(i) arranged so as to correspond to a physical address space,

(ii) each cell having at least one transistor,

(iii) each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., and Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) judging whether a logical address space including the logical address matches the physical address space;

(c) specifying the most significant bit X1 by

(i) applying

1) a predetermined reference voltage

2) to a gate of the transistor

3) to determine whether a current flows between a source and a drain of the transistor.

4) when the logical address space matches the physical address space; and

(d) outputting the specified bit from one of the cells corresponding to the physical address.

ii. 22. A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (Xl, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit Xl by applying a reference voltage to a gate of the transistor when the logical address space matches the physical address space to

determine whether a current flows between a source and a drain of the transistor; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

c. First species (i.e., having a feature of specifying the most significant bit X1 by **comparing** an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space):

i.18 A method

(1) of reading

(a) n (n => 2) number of bits (X1, X2, ..., Xn)

(b) from a plurality of multilevel memory cells

(i) arranged so as to correspond to a physical address space,

(ii) each cell having at least one transistor,

(iii) each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., and Xn),

(2) comprising the steps of:

(a) converting a logical address into a physical address included in the physical address space;

(b) judging whether a logical address space including the logical address matches the physical address space;

(c) specifying the most significant bit X1 by

(i) comparing

1) an output voltage of the transistor corresponding to

2) the most significant bit with a reference voltage

3) when the logical address space matches the physical address space; and

(d) outputting the specified bit from one of the cells corresponding to the physical address.

ii. 24. A computer readable medium storing program code for causing a computer to read n (n => 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

(1) first program code means for converting a logical address into a physical address included in the physical address space;

(2) second program code means for judging whether a logical address space including the logical address matches the physical address space;

(3) third program code means for specifying the most significant bit X1 by comparing an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space; and

(4) fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

10. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, the feature of "specifying the most significant bit X1" is generic.

11. Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

12. Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

13. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

14. During a telephone conversation with Mr. George Pettit, Reg. No. 27,369, on August 11, 2003, a provisional election was made with traverse to prosecute the invention of Group I, claims 6, 7, 26-2-32. Affirmation of this election must be made by applicant in replying to this

Office action. Claims 8-15, 20, 16, 17, 22, 23, 18, 19, 24, 25, 37-42, 33-36 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

DRAWINGS ARE OBJECTED

15. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s):

a. the "first program code" recited in claim 6;

b. the "second program code" recited in claim 6;

c. the "third program code" recited in claim 7;

d. the "fourth program code" recited in claim 7;

e. the "bit disperser" recited in claim 26;

f. the "program code for dispersing" recited in claim 32.

No new matter should be entered..

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

17. Claims 26-29 are rejected under 35 U.S.C. 112, first paragraph, as being directed to a single element device.

i. With regard to claim 26 and thus its dependent claims 27-29:

(1) This claim claims a single element named "a bit disperser for dispersing bits, " and thus rejected under 35 USC 112, first paragraph, according to MPEP section 2164.08(a), which reads as follow:

> **2164.08(a) Single Means Claim**
>
> A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. *In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to *Hyatt* is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

18. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

19. Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. With regard to claim 6:

(1) It is not clear how the phrase "the first and the second data being coded by a coding method", which modifies the first data and the second data, affects the first program code means. Notice that the first program means is for causing a computer to enter at least the first data and the second data, rather than causing the computer to code those data

(2) The clause "at least a bit of an N-order of the first data bits and a bit of the N-order of the second data bits are stored in one of the cells" is confusing in that it is not clear what bit (either of the first data bits or of the second data bits) is stored in which one of the

cells. The Applicant is to clearly recite the meaning of this clause rather, than the clause as it is.

(3) The use of "such that ..." clause is indefinite. In the instant claim, the "such that ..." clause does not specifically indicate to the arranging is so as to affect the intention set forth in the clause.

ii. With regard to claim 7:

(1) The usage of the word "generating" in this claim is vague and indefinite. Notice that it would not be possible for a program code to generate a voltage. Even if the program code is to cause a computer to do it, then still the computer cannot possible generate a voltage of electricity.

Double Patenting

20. Claim 6, 7, and 26-29 are provisionally rejected under the judicially created doctrine of double patenting over claim claims 1-11 of copending Application No. 6,023,781. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as listed herein below:

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

a. As per claim 6:

i. Claim 6 claims a computer readable medium, which computer readable medium is:

(1) storing program code

(2) for causing a computer

(a) to write

(i) data of bits

(ii) in a semiconductor device

1) having a plurality of multilevel memory cells,

I each cell storing at least three levels of data each,

(3) comprising:

(a) first program code means

(i) for entering

1) at least

I a first data composed of a plurality of first data bits and

II a second data composed of a plurality of second data bits,

1} the first and the second data being coded by a coding method; and

(b) second program code means

(i) for arranging

1) the first and the second data bits

2) such that

I **at least**

1} **a bit** of an N-order of the first data bits **and a bit** of the

N-order of the second data bits

3} **are stored** in one of the cells, N being an integral number.

ii. With regard to claim 6:

(1) Claim 5 of patent number 6,023,781 substantially teaches the limitations as claimed in the present claim 7. Notice that the functions of the program code means in the present claim 6 are the steps performed by the method of claim 5 of the patent.

(2) However claim 5 of the patent does not explicitly state that the steps are carried out by a computer as affected by program code means.

(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that operations done on a memory are perform by a computer according to a program instruction codes.

b. As per claim 7:

i. Claim 7 claims:

(1)7. The computer readable medium according to claim 6 further comprising:

(a) third program code means for **generating at least a voltage corresponding to the N-order bits**; and

(b) fourth program code means for **applying the voltage to the one of the cells in response to an address information corresponding to the one of the cells**.

ii. With regard to Claim 7:

(1) Claim 5 of patent number 6,023,781 substantially teaches the limitations as claimed in the present claim 7.

c. As per claim 26:

i. Claim 26 claims:

(1) a semiconductor device that is:

(a) having

(i) a plurality of multilevel memory cells,

1) each cell storing one of at least three levels of data each; and

(b) comprising

(i) a bit disperser for dispersing

1) bits,

I which bits constituting at least one code data coded by a coding method to be stored in the cells,

2) over the plurality of multilevel memory cells

3) to store the bits therein.

ii. With regard to Claim 26:

(1) Claim 1 of patent number 6,023,781 substantially teaches the semiconductor device as claimed. Notice that the bit disperser (in the present claim) reads on the arranging means in claim of the patent.

d. As per claim 27:

i. Claim 27 claims:

(1)27 The semiconductor device according to claim 26, wherein the bit disperser

(a) **controls**

(i) **the number of bits to be stored in at least one of the cells**

(ii) **in accordance with capability of code error correction of the coding method.**

ii. With regard to Claim 27:

(1) Claim 2 of patent number 6,023,781 teaches **controls the number of bits to be stored in at least one of the cells in accordance with capability of code error correction of the coding method.**

e. As per claim 28:

i. Claim 28 claims:

(1)28 The semiconductor device according to claim 26, wherein the bit disperser

(a) puts the bits of M number of code data, each code data having a code length N, into positions of arrangement in M lines x N rows and

(b) stores the M number of bits in each cell, the M and N being an integral number.

ii. With regard to Claim 28:

(1) Claim 3 of patent number 6,023,781 substantially teaches the semiconductor device as claimed. Notice that the bit disperser's

function of arranging (in the present claim) reads on the function of the arranging means in the claim of the patent.

f. As per claim 29:

i. Claim 29 claims:

(1)29 The semiconductor device according to claim 26, wherein the **multilevel memory cells are non-volatile semiconductor memories**.

ii. With regard to Claim 29:

(1) Claim 4 of patent number 6,023,781 substantially teaches the semiconductor device as claimed.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the

United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

22. Claims 26, 29 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Baldi (5,761,222).

a. As per claim 26:

i. Claim 26 claims:

(1) a semiconductor device that is:

(a) having

(i) a plurality of multilevel memory cells,

1) each cell storing one of at least three levels of data each; and

(b) comprising

(i) a bit disperser for dispersing

1) bits, which bits constituting at least one code data coded by a coding method to be stored in the cells,

2) over the plurality of multilevel memory cells

3) to store the bits therein.

ii. With regard to Claim 26:

(1) Baldi teaches [through any of his Figures 1-6]

(a) a semiconductor device which is:

(i) having

1) a plurality of multilevel memory cells [i.e., the cells that are inherent in his DM element, which DM element is of multilevel type (see his Detailed Description Text (DEDT, paragraph 40), for the DM element being multilevel],

I each cell storing one of at least three levels of data each -- [see his DETX, paragraph 8, for the desired number of levels], and

(ii) comprising

1) a bit disperser for dispersing

I bits, which bits constituting at least one code data coded by a coding method to be stored in the cells,

II over the plurality of multilevel memory cells

III to store the bits therein.

2) [which **disperser is inherent in Baldi's semiconductor device because**:

I Baldi mentioned about a writing mechanism that present dispersion in distribution [col. 3, lines 7-10];

II Baldi's multilevel memory cells are "flash-able" (i.e., they are programmed/erased in block manner, and a plurality of cells in a block can be programmed simultaneously, which simultaneousness would require the bits of a code block be distributed/dispersed/broken/scattered to their respective cells) -- [see Baldi's col. 2, lines 21-24, for his Flash EEPROM];

III Baldi:

1} recognized that his Flash EEPROM writing mechanism, which presents dispersion, cause errors due to high speed -- [col. 3, lines 7-13]; and

2} [thus provides his technique for resolving those errors].

b. As per claim 29:

i. Claim 29 claims:

(1)29 The semiconductor device according to claim 26, wherein the **multilevel memory cells are non-volatile semiconductor memories**.

ii. With regard to Claim 29:

(1) Baldi teaches

(a) that his **multilevel memory cells [i.e., the cells in element DM (i.e., the first memory means --col. 11, lines 1-2; lines 43-46]] are non-volatile semiconductor memories [since DM is of EEPROM type (col. 11, lines 48-51)]**.

c. As per claim 31:

i. Claim 31 claims a method:

(1) of writing

(a) at least one code data coded by a coding method

(b) in a semiconductor device

(i) having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each,

(2) comprising the step of

(a) dispersing

(i) bits constituting the code data

(ii) over the plurality of multilevel memory cells.

ii. With regard to Claim 31:

(1) This claim recited the function of the bit disperser of claim 26 rejected above. This claim is thus has limitation that is similar to that of claim 26. This claim is thus rejected with the same rationale applied against claim 26.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 27, 28, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldi (5,761,222) in view of common practice in the art.

a. As per claim 27:

i. Claim 27 claims:

(1)27 The semiconductor device according to claim 26, wherein the bit disperser

(a) **controls**

(i) **the number of bits to be stored in at least one of the cells**

(ii) **in accordance with capability of code error correction of the coding method.**

ii. With regard to Claim 27:

(1) Official notice is hereby taken that:

(a) using a combination of memory patching (i.e., using alternative/redundant memory cells to replace defective memory cells) and error correction code (ECC) is notoriously old and well known in the art of memory accessing control.

(2) It would have been obvious for a person having ordinary skill in the art at the time the invention was made to:

(a) first, use error correction code (ECC) to store with its corresponding data to store the ECC and its data in a memory block; and

(b) second, if the memory block has to many defective cells (beyond the error correction capability of the ECC) then use replacement cells to replace those defective cells and to store the data bits in those replacement cells.

(3) In view of memory patching, which is notoriously old and well known in the art, a skilled person in the art would have realize the a dispersing/distributing controller would be programmed to control

the number of bits in a set of data in such a manner so that those bits in the set of data can be directed to replacement cells and be stored therein instead of storing them in the defective areas which cannot be corrected by using ECC.

b. As per claim 28:

i. Claim 28 claims:

(1)28 The semiconductor device according to claim 26, wherein the bit disperser

(a) puts the bits of M number of code data, each code data having a code length N, into positions of arrangement in M lines x N rows and

(b) stores the M number of bits in each cell, the M and N being an integral number.

ii. With regard to Claim 28:

(1) Baldi teaches:

(a) that his memory DM:

(i) is of Flash EEPROM type [col. 2, line 62; col. 6, line 28; col. 11, line 49];

(ii) is multilevel; and

(iii) is an array of memory cells [col. 8, lines 25-26].

(2) However Baldi does not explicitly mention about

(a) putting the bits of M number of code data, each code data having a code length N, into positions of arrangement in M lines x N rows and

(b) storing the M number of bits in each cell,

(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(a) realize that in programming/writing/flashing Baldi's Flash EEPROM it would be obvious to do a combination of **putting the bits of M number of code data, each code data having a code length N, into positions of arrangement in M lines x N rows and storing the M number of bits in each cell**.

(4) The skilled person would have been motivated to come to this realization because such manner in which a Flash EEPROM is flashed is notoriously old and well known in the art -- [the manner is that Flash EEPROM is programmable in block of arrayed cells].

c. As per claim 30:

i. Claim 30 claims:

(1) A computer readable medium

(a) storing program code

(b) for causing a computer to store

(i) data

(ii) in a semiconductor device

1) having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each,

(c) comprising

(i) a program code means

1) for dispersing

I bits, which bits constituting at least one code data coded by a coding method to be stored in the cells,

II over the plurality of multilevel memory cells

III to store the bits therein.

ii. With regard to claim 30:

(1) Baldi (5,761,222) teaches [at col. 1, lines 49-53; col. 3, lines 7-9]

(a) dispersing [see Figure 3, 4, 5 or 6; (see also col. 3, lines 7-17, for the dispersion)]

(i) data [i.e., DI], [which code data has inherently been coded by certain coder according to certain coding method],

(ii) over cells in a semiconductor device [i.e., Figure 1] having

1) a plurality of multilevel memory cells [see Abstract, line 2; col. 1, lines 17, 64; col. 2, lines 2, 58-65],

I each of which cells storing one of at least three levels of data each [col. 2, lines 57-61],

(iii) [which writing is inherently done by a computer using Baldi's semiconductor device].

(2) However, Baldi does not explicitly teach:

(a) a program code which cause a computer to do such dispersing/writing.

(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(a) realize that the computer, in which Baldi's a semiconductor device is used, would be controlled by a program code in order to do its operation in dispersing the code data bits.

(4) The skilled person would have been motivated to:

(a) realize this because it is a common knowledge in the art of writing/programming data bits into a memory requires a program code written to control a computer to do the writing/programming and which writing/programming would require the bits to be distributed/dispersed/scattered/arranged so as to be stored/programmed/written into the cells of the memory.

d. As per claim 32:

i. Claim 32 claims a computer readable medium

(1) storing program code

(2) for causing a computer to write

(a) at least one code data coded by a coding method

(b) in a semiconductor device

(i) having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each,

(3) comprising

(a) the program code

(i) for dispersing

1) bits constituting the code data

2) over the plurality of multilevel memory cells.

ii. With regard to claim 32:

(1) Baldi (5,761,222) teaches [at col. 1, lines 49-53; col. 3, lines 7-9]

(a) dispersing [see Figure 3, 4, 5 or 6; (see also col. 3, lines 7-17, for the dispersion)]

(i) at least one code data [i.e., DI], [which code data has inherently been coded by certain coder according to certain coding method],

(ii) over cells in a semiconductor device [i.e., Figure 1] having

1) a plurality of multilevel memory cells [see Abstract, line 2; col. 1, lines 17, 64; col. 2, lines 2, 58-65], each of which cells storing

one of at least three levels of data each [col. 2, lines 57-61],

(iii) [which writing is inherently done by a computer using Baldi's semiconductor device].

(2) However, Baldi does not explicitly teach:

(a) a program code which cause a computer to do such dispersing/writing.

(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(a) realize that the computer, in which Baldi's a semiconductor device is used, would be controlled by a program code in order to do its operation in dispersing the code data bits.

(4) The skilled person would have been motivated to:

(a) realize this because it is a common knowledge in the art of writing/programming data bits into a memory requires a program code written to control a computer to do the writing/programming and which writing/programming would require the bits to be distributed/dispersed/scattered/arranged so as to be stored/programmed/written into the cells of the memory.

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

26. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sheikh, Ayaz, can be reached on (703) 305-9648. The fax phone number for this Group is (703) 305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

LY V. HUA
PRIMARY PATENT EXAMINER
ART UNIT 2131

L. Hua
August 18, 2003